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DB=PGPB,USPT; PLUR=YES; OP=ADJ

<u>L63</u>	L59 near cluster
<u>L62</u>	L59 near bundle
<u>L61</u>	L59 near group
<u>L60</u>	L59 and card near group near fiber adj channels
<u>L59</u>	management adj processor
<u>L58</u>	L57 and cards
<u>L57</u>	L47 and backplane near cluster
<u>L56</u>	L47 and backplane near bundle
<u>L55</u>	L47 and backplane near group

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<u>L54</u>	L53 and routing	17	<u>L54</u>
<u>L53</u>	L52 and cards	30	<u>L53</u>
<u>L52</u>	L47 and cluster	30	<u>L52</u>
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<u>L49</u>	L47 and bundle	7	<u>L49</u>
<u>L48</u>	L47 and bundles	7	<u>L48</u>
<u>L47</u>	management adj processor and backplane	136	<u>L47</u>
<u>L46</u>	management adj processor and modules and group near interconnect	0	<u>L46</u>
<u>L45</u>	management adj processor and cards and group near interconnect	0	<u>L45</u>
<u>L44</u>	L42 and modules	0	<u>L44</u>
<u>L43</u>	L42 and cards	1	<u>L43</u>
<u>L42</u>	management adj processor near route	2	<u>L42</u>
<u>L41</u>	management adj processor near routing	1	<u>L41</u>
<u>L40</u>	L38 and route	7	<u>L40</u>
<u>L39</u>	L38 and routing	2	<u>L39</u>
<u>L38</u>	management adj processor and plurality adj cards	16	<u>L38</u>
<u>L37</u>	L36 and routing near information	1	<u>L37</u>
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<u>L35</u>	L34 and plurality near card	1	<u>L35</u>
<u>L34</u>	L33 and backplane	30	<u>L34</u>
<u>L33</u>	cluster and management adj processor	113	<u>L33</u>
<u>L32</u>	data adj interconnect and cluster and management adj processor	1	<u>L32</u>
<u>L31</u>	data adj interconnect and bundle and management adj processor	0	<u>L31</u>
<u>L30</u>	L29 and routing	1	<u>L30</u>
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<u>L27</u>	management adj processor and plurality adj modules	9	<u>L27</u>
<u>L26</u>	L19 and interconnect	1	<u>L26</u>
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<u>L23</u>	L21 and inteconnect	0	<u>L23</u>
<u>L22</u>	L19 and backplane	1	<u>L22</u>
<u>L21</u>	L20 and backplane	7	<u>L21</u>
<u>L20</u>	L14 and route	7	<u>L20</u>
<u>L19</u>	L14 and routing	2	<u>L19</u>
<u>L18</u>	L14 and routing adj data	0	<u>L18</u>
<u>L17</u>	L14 and route adj information	0	<u>L17</u>
<u>L16</u>	L14 and routing adj information	0	<u>L16</u>
<u>L15</u>	L14 and routing adj information	0	<u>L15</u>
<u>L14</u>	management adj processor and plurality adj cards	16	<u>L14</u>

DB=USPT; PLUR=YES; OP=ADJ

<u>L13</u>	L10a and back-plane	0	<u>L13</u>
<u>L12</u>	L10 and backplane	0	<u>L12</u>
<u>L11</u>	L10 and route	0	<u>L11</u>
<u>L10</u>	L9 and routing	1	<u>L10</u>
<u>L9</u>	management adj processor and plurality adj cards	4	<u>L9</u>
<u>L8</u>	management adj processor and multiple adj cards	1	<u>L8</u>
<u>L7</u>	L1 and management adj processor	1	<u>L7</u>
<u>L6</u>	L3 and management adj processor	0	<u>L6</u>
<u>L5</u>	L4 and management adj processor	0	<u>L5</u>
<u>L4</u>	L3 and cluster	1	<u>L4</u>
<u>L3</u>	L2 and group	2	<u>L3</u>
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Relevance scale ☐ ☐ ☐ ☐ ☐1 [Experiences of building an ATM switch for the local area](#)

Richard Black, Ian Leslie, Derek McAuley

 October 1994 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Communications architectures, protocols and applications**, Volume 24 Issue 4

Full text available: pdf (1.12 MB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The Fairisle project was concerned with ATM in the local area. An earlier paper [9] described the preliminary work and plans for the project. Here we present the experiences we have had with the Fairisle network, describing how implementation has changed over the life of the project, the lessons learned, and some conclusions about the work so far.

2 [Development of processors and communication networks for embedded systems: Component-based design approach for multicore SoCs](#)

W. Cesário, A. Baghdadi, L. Gauthier, D. Lyonnard, G. Nicolescu, Y. Paviot, S. Yoo, A. A. Jerraya, M. Diaz-Nava

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf (187.82 KB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper presents a high-level component-based methodology and design environment for application-specific multicore SoC architectures. Component-based design provides primitives to build complex architectures from basic components. This bottom-up approach allows design-architects to explore efficient custom solutions with best performances. This paper presents a high-level component-based methodology and design environment for application-specific multicore SoC architectures. The system speci ...

Keywords: HW/SW interfaces abstraction, component-based design, multicore System-on-Chip

3 [The muse object architecture: a new operating system structuring concept](#)Yasuhiko Yokote, Fumio Teraoka, Atsushi Mitsuzawa, Nobuhisa Fujinami, Mario Tokoro
April 1991 **ACM SIGOPS Operating Systems Review**, Volume 25 Issue 2

Full text available: pdf (1.92 MB)

 Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

A next generation operating system should accommodate an ultra large-scale, open, self-


advancing, and distributed environment. This environment is dynamic and versatile in nature. In it, an unlimited number of objects, ranging from fine to coarse-grained, are emerging, vanishing, evolving, and being replaced; computers of various processing capacities are dynamically connected and disconnected to networks; systems can optimize object execution by automatically detecting the user's and/or program ...

4 BIST TPG for faults in system backplanes

Chen-Huan Chiang, Sandeep K. Gupta

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available:  [pdf \(108.29 KB\)](#)

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Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A built-in self-test (BIST) methodology to test system backplanes by using BIST functionality in each of its constituent boards is presented. Since the configurations of systems change frequently, at the system level, the proposed methodology employs a simple test schedule which can be easily changed whenever the system configuration is changed. Since the boards used in such systems are designed for use in a wide variety of systems, the proposed methodology defines the test objectives to be achieved ...

Keywords: BIST circuit, BIST methodology, VME backplane, built-in self test, built-in self-test, edge pin connections, programmable test architecture, simple test schedule, system backplanes, system configuration

5 Pin assignment of circuit cards and the routability of multilayer printed wiring backplanes

Hing C. So

June 1973 **Proceedings of the 10th workshop on Design automation**

Full text available:  [pdf \(793.72 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper examines the relationship between the pin assignment for circuit cards and the routability of the multilayer printed wiring backplane on which the cards are mounted. It is shown that the pin assignment should meet three objectives in order to facilitate backplane routing. Heuristic strategies for determining a pin assignment to attain these objectives are given. These strategies have been implemented in a program which was used in two separate experiments involving two different ...

6 Scheduling Optimization on the Simbus Backplane

Dale E. Martin, Philip A. Wilsey, Robert J. Hoekstra, Eric R. Keiter, Scott A. Hutchinson, Thomas V. Russo, Lon J. Waters

April 2004 **Proceedings of the 37th annual symposium on Simulation**

Full text available:  [pdf \(131.58 KB\)](#)

Additional Information: [full citation](#), [abstract](#)


Continuous system models are becoming increasingly more important in the modeling and analysis of complex systems. Unfortunately, the runtime simulation costs required to support continuous modeling can be prohibitive to their use. One technique to decrease simulation runtime costs is mixed-domain simulation where the system is modeled by a mixture of discrete and continuous elements. In those regions where highly detailed information is required, continuous models can be used, and discrete models can be used ...


7 ABLE: AMD backplane for layout engines

Kenneth W. Wan, Roshan A. Gidwani


July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available:  [pdf\(595.16 KB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

- 8 [The design of nectar: a network backplane for heterogeneous multicomputers](#) 
Emmanuel Arnould, H. T. Kung, Francois Bitz, Robert D. Sansom, Eric C. Cooper
April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems**, Volume 17 Issue 2


Full text available:  [pdf\(1.73 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Nectar is a "network backplane" for use in heterogeneous multicomputers. The initial system consists of a star-shaped fiber-optic network with an aggregate bandwidth of 1.6 gigabits/second and a switching latency of 700 nanoseconds. The system can be scaled up by connecting hundreds of these networks together. The Nectar architecture provides a flexible way to handle heterogeneity and task-level parallelism. A wide variety of machines can be connected as Nectar nodes ...

- 9 [A router for multilayer printed wiring backplanes](#) 
J. C. Foster
June 1973 **Proceedings of the 10th workshop on Design automation**

Full text available:  [pdf\(383.69 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)





Multilayer printed wiring backplanes cause a special problem for design automation. The very size of the problem tends to make routing techniques which are satisfactory for smaller boards prohibitively expensive for larger ones. At the same time, however, the following factors make it mandatory that adequate computer routing exist. 1. The number of connections to make, the number of layers available and the ability to use vias makes the problem too complex for manual routing.

- 10 [Symphony: a simulation backplane for parallel mixed-mode co-simulation of VLSI systems](#) 
Antonio R. W. Todesco, Teresa H.-Y. Meng
June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available:  [pdf\(73.19 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

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1 **Product distribution: The transshipment problem**

John B. Vinturella

August 1972 **Proceedings of the ACM annual conference - Volume 2**

Full text available: pdf(388.22 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The common-carrier distribution network for the Luzianne food product line is discussed, along with modifications under consideration. Considerations governing the design of a simulation model of the network are enumerated. The Distribution Simulator (DSIM) developed for this application is then described and early computational experience included.

Keywords: Common-carrier, Data management, Distribution, Routing, Simulation, Transportation problem, Transshipment

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